Yuan Hsi (Tommy) Chou

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Education

University of British Columbia
Ph.D. Candidate in Electrical and Computer Engineering Expected 2024
Current research: GPU ray tracing acceleration
Supervisor: Dr. Tor M. Aamodt

University of Michigan, Ann Arbor
Master of Science in Engineering, Electrical and Computer Engineering April 2019
Coursework: Integrated Circuits & VLSI GPA: 3.79/4.00

University of Texas, Austin
Bachelor of Science in Engineering in Electrical & Computer Engineering May 2017
Coursework: Integrated Circuits, VLSI, Digital Signal Processing GPA: 3.52/4.00

Publications

[1] M. Saed, Y. Chou, L. Liu, T. Nowicki, and T. M. Aamodt, "Vulkan-Sim: A GPU Architecture Simulator for Ray Tracing, " IEEE/ACM International Symposium on Microarchitecture (MICRO), 2022.
[2] M. Saed, **Y. Chou**, L. Liu, T. Nowicki, and T. M. Aamodt, "Vulkan-Sim: A GPU Architecture Simulator for Ray Tracing, " IEEE/ACM International Symposium on Microarchitecture (MICRO), 2022.
[3] L. Liu, W. Chang, F. Demoullin, **Y. Chou**, M. Saed, D. Pankratz, T. Nowicki, T. Aamodt, "Intersection Prediction for Accelerated GPU Ray Tracing, " IEEE/ACM International Symposium on Microarchitecture (MICRO), 2021
[4] **Y. H. Chou**, C. Ng, S. Cattell, J. Intan, M. D. Sinclair, J. Devietti, et al., "Deterministic atomic buffering", IEEE/ACM International Symposium on Microarchitecture (MICRO), 2020
[5] **Y. H. Chou** and S. L. Lu, "A High Performance, Low Energy, Compact Masked 128-Bit AES in 22nm CMOS Technology, " International Symposium on VLSI Design, Automation and Test (VLSI-DAT), 2019.
[6] **Y. H. Chou**, T.L. Hsieh, C.Y. Tsai, C.C. Wang, L.T. Hwang, "An Ultra Low Loss SerDes Signal Design on a FC Package Applied in 56Gbps Networks, " IEEE Electronic Components and Technology Conference, 2016
[7] S.C. Hsieh, C.Y. Kung, T.C. Lee, C.H. Chen, C.C. Wang, **Y.H. Chou** "Compact Size and Low Profile IPD Diplexer Design Applied on Wireless Module of Mobile Phone, " International Conference on Electronic Packaging Technology, 2016

Skills

Programming Languages	C, C++, Verilog, Python, MATLAB
Graphics APIs	Vulkan, OpenGL
Architectural Simulators	GPGPU-Sim
Hardware Design Tools	Virtuoso, VCS, Innovus, Design Compiler, HSPICE, CustomSim, ModelSim, Quartus, HFSS
Spoken Languages	English, Mandarin

Work Experience

Huawei Research Center, Vancouver, Canada
Associate Engineer, Intern May 2021 – Aug 2021

- Improved denoiser quality and performance for ambient occlusion, reflection, and caustics effects in a hybrid renderer (rasterization + ray tracing) using Vulkan API

University of British Columbia, Vancouver, Canada
Graduate Research Assistant June 2019 – Now

- PhD student supervised by Dr. Tor M. Aamodt
- Research area in GPU graphics, ray tracing acceleration, and hardware modeling/simulation
- "Deterministic Atomic Buffering" published in MICRO 2020

- "Intersection Prediction for Accelerated GPU Ray Tracing" accepted in MICRO 2021

Teaching Assistant Sept 2019 – Now
- Teaching assistant for CPEN 211 (2019, 2020), CPEN 311 (2019, 2020, 2021, 2022), CPEN 391 (2021)

Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan
Intern – Design Technology Platform (DTP) June 2018 – August 2018
- Designed a high performance compact masked AES core in TSMC 22nm technology
- Performed DPA and CPA side channel attacks on the implemented design with CustomSim simulation
- Research paper accepted in VLSI-DAT 2019 conference

Advanced Semiconductor Engineering Inc. (ASE), Kaohsiung, Taiwan
Intern - RF Design Team June 2016 – August 2016
- Designed low loss baluns through HSPICE and 3D EM simulations
- Studied trends on front end modules for mobile devices based on market research and technology analysis reports
- Received outstanding paper award on a submission to ICEPT 2016

Intern - Electrical Lab May 2015 – August 2015
- Developed a trace structure used in flip chip packaging that achieved low insertion loss at high frequencies
- Conducted 3D EM simulations with ANSYS HFSS, Q3D, SIwave on chip packages
- Research paper accepted in IEEE ECTC 2016 conference

Intern - Stress-Thermal Lab May 2014 – August 2014
- Performed thermal stress tests on packaged chips for estimating device lifetime
- Assisted with data analysis and making experiment reports
- Translated technical documents from English to Mandarin

Related Coursework

University of Michigan, Ann Arbor
EECS 627 – VLSI Design II
High Performance AES Engine with Side Channel Protection
- Designed a highly pipelined AES engine with side channel protection using RDVFS in Verilog
- Completed VLSI design flow from Verilog to synthesis to APR using industrial tools

EECS 570 – Parallel Computer Architecture
Parallel Banded Smith-Waterman Accelerator
- Designed a compact parallel banded Smith-Waterman accelerator based on systolic array for genome sequencing
- Achieved significant power and area advantage over GPUs in global alignment for genome sequencing applications

EECS 425 – Integrated Microsystem Laboratory
3-Axis Force Balanced Accelerometer Using a Single Proof-Mass
- Designed and fabricated a 3-axis accelerometer MEMS sensor in COMSOL with SoG technology
- Designed and fabricated a sigma-delta modulation interface circuit in Cadence with ED-NMOS technology

EECS 427 – VLSI Design I
DICE-SECDED Based Reliable Register File
- Designed a 16x16 resilient register file using DICE and SECDED techniques from reading research papers
- Completed layout and characterization of the register file in Virtuoso

EECS 470 – Computer Architecture
P6 Style Out of Order 3 Way Superscalar RISC Processor
- Implemented a 3 way superscalar out of order processor in P6 style in Verilog
- Includes features such as store to load forwarding, next-line prefetching and victim cache to increase performance

University of Texas, Austin

Senior Design Project - ATE to Verilog Translator

- Created a bidirectional software language translator between C++ and Verilog-AMS using a Python script
- Established the connection between Texas Instruments Teradyne Eagle ATE test programs and Verilog simulations for consistency in design and verification
- Worked in a student team in collaboration and mentored by Texas Instruments

EE 460M - Digital Systems Design Using HDL

- Implemented and modified a MIPS processor with Verilog on a FPGA
- Worked with IO interfaces such as USB and VGA to communicate with a FPGA

EE 445S - Real-Time Digital Signal Processing Laboratory

- C programming and measurement of communication and DSP systems through a DSP chip with the use of oscilloscope
- Theory and implementation of sinusoidal wave generation, FIR and IIR filters, PN sequences and data scramblers, PAM and QAM data transmission and reception